APPEAL BRIEF
EMC-01-102CIP1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL BRIEF ON BEHALF OF MICHAEL KOWALCHIK, ET AL.

PURSUANT TO 37 C.F.R. 41.31

APPLICANT:	Michael Kowalchik, et al	*GROUP ART UNIT:*	2189
U.S.S.N.:	10/731,622	*CONFIRMATION NO.:*	**4760**
FILING DATE:	December 9, 2003	*EXAMINER:*	Chace, Christian
		CUSTOMER NO.	**24227**
TITLE:	*DATA STORAGE DEVICE*		

CERTIFICATE OF FACSIMILE UNDER 37 C.F.R. §1.8(a)

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APPEAL BRIEF

This is an Appeal Brief in connection with an Appeal from a final rejection decision of the Primary Examiner dated June 27, 2006 in the above-identified application and pursuant to a Notice of Appeal filed on October 27, 2006. This Appeal Brief is being filed with a Petition for a Two Month Extension of Time pursuant to 37 C.F.R. 41.31 and 37 CFR 1.136.

page 31 to 46 are US patent and are recycled.

Applicant: Michael Kowalchik, *et al.*
U.S.S.N.: 10/731,622
Filing Date: December 9, 2003
EMC Docket No.: EMC-01-102CIP1

APPEAL BRIEF

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I. REAL PARTY IN INTEREST

The real party in interest is EMC Corporation, the assignee of record.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF CLAIMS

Claims 30-50 are on appeal.

Claim 30 is rejected.

Claim 31 is rejected.

Claim 32 is rejected.

Claim 33 is canceled.

Claim 34 is rejected.

Claim 35 is rejected.

Claim 36 is rejected.

Claim 37 is rejected.

Claim 38 is rejected.

Claim 39 is rejected.

Claim 40 is rejected.

Claim 41 is rejected.

Claim 42 is rejected.

Claim 43 is rejected.

Claim 44 is canceled.

Claim 45 is rejected.

Claim 46 is canceled.

Claim 47 is rejected.

Claim 48 is rejected.

Claim 49 is rejected.

Claim 50 is rejected.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent Claim 30

Independent claim 30 is directed to a data storage device 300, Fig. 13, comprising a device interface for receiving data access requests (The preliminary amendment filed on December 9, 2003 ("Prelim"), describes the device interface provided by controller 304 (Fig. 13) on page 5 lines 28-29. The application specification ("Specification") describes the data requests 250-256, Figs. 2-5, on page 7, lines 25-26). The system includes a device housing 306, Fig. 13, conforming to a standard form factor (Prelim page 5, lines 16-18); a plurality of non-volatile memory devices 302a-302n, Fig. 13 (Prelim page 5, lines 13-25); and a controller 304 that accesses the non-volatile memory devices in response to the received data access requests (Prelim page 5, lines 28-29; Specification page 7, line 24 – page 8, line 19).

The plurality of non-volatile memory devices 302a-302n are selected from the group consisting of flash memory; compact flash memory; magnoresistive RAM; ferroelectric RAM; dynamic RAM and static RAM being maintained as non-volatile with the use of a power subsystem and microelectromechanical memory devices (Prelim page 5, lines 20-25.).

Independent Claim 43

Independent claim 43 is directed to a data storage device 114, Fig. 7, comprising a first data storage device having a platter size of at least 3.5 inches in diameter (Specification page 8, lines 26-29, element 100a-100n, Fig. 7). The system includes a second data storage device 106, Fig. 7, 300, Fig. 13, having a device interface for receiving data access requests (Prelim, page 5 lines 28-29, describes the device interface provided by controller 304, Fig. 13. Specification, page 7, lines 25-26, describes the data requests 250-256, Figs. 2-5.). The system includes a device housing 306, Fig. 13, conforming to a standard form factor (Prelim page 5, lines 16-18); a plurality of non-volatile memory devices 302a-302n, Fig. 13 (Prelim page 5, lines 13-25); and a first controller 304 configured to receive data access requests from the device interface (Prelim page 5, lines 28-29; Specification page 7, line 24 – page 8, line 5). The system further includes a second controller 116, Fig. 7, that coordinates data access to the at least one first data storage device 100a-100n and the at least one second data storage device 106, 300 (Specification page 8, line 30 – page 9, line 17).

The plurality of non-volatile memory devices 302a-302n are selected from the group consisting of flash memory; compact flash memory; magnoresistive RAM; ferroelectric RAM; dynamic RAM and static RAM being maintained as non-volatile with the use of a power subsystem and microelectromechanical memory devices (Prelim page 5, lines 20-25.).

Independent Claim 45

Independent claim 45 is directed to a method of servicing data access requests at a data storage device, comprising receiving data access requests at a device interface of the data storage device 304, Fig. 13 (Prelim, page 5 lines 28-29, describes the device interface provided by controller 304, Fig. 13. Specification, page 7, lines 25-26, describes the data requests 250-256, Figs. 2-5 received at the device interface.). The method also includes accessing a plurality of non-volatile memory devices housed within a standard form factor housing in response to the received data access requests (Accessing the non-volatile memory devices in response to the received data access requests is disclosed at Prelim page 5, lines 10-29; Specification page 7, line 24 – page 8, line 19.).

The plurality of non-volatile memory devices 302a-302n are selected from the group consisting of flash memory; compact flash memory; magnoresistive RAM; ferroelectric RAM; dynamic RAM and static RAM being maintained as non-volatile with the use of a power subsystem and microelectromechanical memory devices (Prelim page 5, lines 20-25.).

Independent Claim 47

Independent claim 47 is directed to a data storage device comprising a device interface for receiving data access requests (Prelim, page 5 lines 28-29, describes the device interface provided by controller 304, Fig. 13. Specification, page 7, lines 25-26, describes the data requests 250-256, Figs. 2-5.). The system includes a plurality of non-volatile memory devices 302a-302n, Fig. 13 (Prelim page 5, lines 13-25); and a controller 304 that accesses the non-volatile memory devices in response to the received data access requests (Prelim page 5, lines 28-29; Specification page 7, line 24 – page 8, line 5.). The controller is configured to implement a RAID scheme (Specification page 6, line 16 – page 7, line 23.).

The plurality of non-volatile memory devices 302a-302n are selected from the group consisting of flash memory; compact flash memory; magnoresistive RAM; ferroelectric RAM;

dynamic RAM and static RAM being maintained as non-volatile with the use of a power subsystem and microelectromechanical memory devices (Prelim page 5, lines 20-25.).

Independent Claim 49

Independent claim 49 is directed to a data storage device comprising a device interface for receiving data access requests (Prelim, page 5 lines 28-29, describes the device interface provided by controller 304, Fig. 13. Specification, page 7, lines 25-26, describes the data requests 250-256, Figs. 2-5). The system includes a plurality of non-volatile memory devices 302a-302n, Fig. 13 (Prelim page 5, lines 13-25); and a controller 304 that accesses the non-volatile memory devices in response to the received data access requests (Prelim page 5, lines 28-29; Specification page 7, line 24 – page 8, line 5.).

The plurality of non-volatile memory devices 302a-302n are selected from the group consisting of flash memory; compact flash memory; magnoresistive RAM; ferroelectric RAM; dynamic RAM and static RAM being maintained as non-volatile with the use of a power subsystem and microelectromechanical memory devices (Prelim page 5, lines 20-25.).

Independent Claim 50

Independent claim 50 is directed to a data storage device comprising a device interface for receiving data access requests (Prelim, page 5 lines 28-29, describes the device interface provided by controller 304, Fig. 13. Specification, page 7, lines 25-26, describes the data requests 250-256, Figs. 2-5.). The system includes a plurality of non-volatile memory devices 302a-302n, Fig. 13 (Prelim page 5, lines 13-25); and a controller 304 that accesses the non-volatile memory devices in response to the received data access requests (Prelim page 5, lines 28-29; Specification page 7, line 24 – page 8, line 5.). The controller is configured to access the non-volatile memory devices in a manner that emulates access to a single disk drive (Specification page 6, lines 1-9.).

The plurality of non-volatile memory devices 302a-302n are selected from the group consisting of flash memory; compact flash memory; magnoresistive RAM; ferroelectric RAM; dynamic RAM and static RAM being maintained as non-volatile with the use of a power subsystem and microelectromechanical memory devices (Prelim page 5, lines 20-25.).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 30-32, 34-43, 45 and 47-50 are unpatentable under 35 U.S.C. §103(a) over Brandt et al. (U.S. Patent No. 5,805,787) in view of Rao (U.S. Patent No. 5,845,104).

VII. ARGUMENT

REJECTION UNDER 35 U.S.C. §103(a) OVER BRANDT IN VIEW OF RAO

Claims 30-32, 34-42, 45 and 47-50

Claims 30-32, 34-42, 45 and 47-50 stand rejected under 35 U.S.C. §103(a) as being unpatentable over by Brandt et al. (U.S. Patent No. 5,805,787) in view of Rao (U.S. Patent No. 5,845,104). The examiner states that, although Brandt does not teach non-volatile memory devices, Rao does, and therefore, it would have been obvious to utilize the flash memory of Rao in the system of Brandt. This rejection is appealed because both Brandt and Rao teach against the combination suggested by the examiner and because the combination suggested by the examiner is based on improper hindsight reconstruction.

In the examiner's comments in Section 11 of the Advisory Action of November 10, 2005, the examiner stated that he did not agree that Brandt teaches away from using flash memory, as he believes that "there are as many reasons to use it as not." The examiner further stated, "It is merely a design choice based on the considerations so well known to those of even rudimentary skill in the art such as cost, size, speed, etc. Brandt simply chose the cheaper route."

However, applicant respectfully asserts that the examiner seems to be ignoring the direct intent and teaching of Brandt. Generally, Brandt's system derives its advantages from the fact that it utilizes inexpensive disk drives as opposed to expensive solid state devices. Brandt discusses the fact that the cost reduction of manufacturing disk drives has far outpaced the cost reductions associated with solid state devices. Column 1, lines 39-42. Brandt states that his invention "advantageously utilizes an array of relatively slow devices, such as low cost disk drives...." Column 2, lines 38-39.

Specifically, Brandt teaches, in Column 6, lines 3-6, that his system "*is an improvement over* directly coupling host 10 to the high volume data storage subsystem 25, or *using a solid state type device, such as caching through the use of a RAM for such interfacing.*" (Emphasis added). Brandt's intent with his invention is to maximize the highest throughput performance *at the least cost* between a host computer and a mass storage system (See the Abstract, lines 2-4). Brandt states that, with this approach, "the high cost of solid state interfacing is significantly

avoided by a large margin..." (Column 6, lines 9-11). Clearly, Brandt teaches the advantage of his device as being its use of relatively slow and inexpensive devices.

To the contrary, Rao teaches, in Column 8, line 39, that flash memory is "*expensive*". Brandt also notes that solid state storage, such as RAM, is expensive. Brandt Column 1, lines 65-66. Given that Brandt's intent is to maximize the highest throughput performance *at the least cost*, and both Rao and Brandt teach that flash memory is expensive, there can be no motivation to combine the teachings of these references. Therefore, based on the teachings of Brandt and of Rao, one of ordinary skill in the art would be specifically *discouraged* from replacing Brandt's multiple disk drives with non-volatile, solid state memory devices.

In establishing a *prima facie* case of obviousness under 35 USC 103, it is incumbent upon the Examiner to provide a "clear and particular" showing of "actual evidence" of a suggestion, teaching, or motivation to combine references. In re Dembiczak, 50 USPQ 2d, 1614, 1617 (Fed. Cir. 1999). "Broad conclusory statements regarding the teachings of multiple references, standing alone, are not evidence." Id., citing McElmury v. Arkansas Power and Light Co., 995 F.2d 1576, 1578, 27 USPQ2d. 1129, 1131 (Fed. Cir. 1993) (internal quotations omitted).

In the rejection, the examiner has broadly stated that Brandt teaches multiple disk drives, that Rao teaches the use of flash memory and that, based on ordinary skill in the art, it would be obvious to combine the two references to come up with applicants' invention. The examiner has not specified any teaching in either reference that would support this combination. Furthermore, the examiner seems to have ignored Brandt's direct teaching *against* the use of solid state memory, with this teaching against being supported by Rao.

In In re Dembiczak, the Court of Appeals for the Federal Circuit recognized that "rigorous application" of the requirement for a showing of a teaching or motivation to combine references is the "best defense against the subtle but powerful attraction" of improper hindsight-based obvious analysis. Id.; See also, Para-Ordnance Manufacturing, Inc. v. SGS Importers International, Inc., 73 F.3d 1085, 37 USPQ2d 1237 (Fed. Cir. 1995). ("obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor"). This is especially true in cases where the ease with which the invention may be understood "may prompt one to fall victim to the insidious effect of hindsight syndrome wherein that which only the inventor taught is used against its teacher." Id. citing W.L. Gore & Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 313 (Fed. Cir. 1983).

The examiner states that even one of rudimentary skill in the art would see that the type of memory used in Brandt is a design choice. However, the examiner has not provided any evidence in either reference or any documentary evidence to prove that, based on the teachings of Brandt and Rao, that that is the case. Only applicants' disclosure teaches the use of non-volatile memory devices in a data storage device as recited in applicants' claims. Accordingly, the only support for the examiner's position the applicants' disclosure, thus rendering the combination relied upon by the examiner as being improperly based hindsight reconstruction. And, as set forth above, this still ignores the fact that both Brandt and Rao teach away from the combination proposed by the examiner.

Accordingly, because Brandt teaches away from utilizing any type of flash, RAM or other type of solid state memory that is not a disk drive because it is not relatively slow and inexpensive, because both Rao and Brandt support the conclusion that flash memory is expensive, and because the only basis for the combination proposed by the examiner is improper hindsight reconstruction, applicants respectfully assert that the 35 U.S.C. §103(a) rejection of independent claims 30, 45, 47, 49 and 50 is improper as being based on an improper combination of references.

Applicants therefore respectfully assert that independent claims 30, 45, 47, 49 and 50 are allowable over the cited art of record and that the 35 U.S.C. §103(a) rejection of independent claims 30, 45, 47, 49 and 50 should be withdrawn.

Claims 31 and 35-42 depend from independent claim 30 and are allowable for at least the same reasons as independent claim 30. Claim 48 depends from independent claim 47 and is allowable for at least the same reasons as independent claim 47.

Claim 43

Claims 43 stands rejected under 35 U.S.C. §103(a) as being unpatentable over by Brandt et al. (U.S. Patent No. 5,805,787) in view of Rao (U.S. Patent No. 5,845,104). The examiner states that Brandt teaches all of the elements of the claim except for the use of non-volatile memory devices selected from the group consisting of flash memory; compact flash memory; magnoresistive RAM; ferroelectric RAM; dynamic RAM and static RAM being maintained as non-volatile with the use of a power subsystem and microelectromechanical memory devices. The examiner states that, although Brandt does not teach non-volatile memory devices, Rao

does, and therefore, it would have been obvious to utilize the flash memory of Rao in the system of Brandt. This rejection is appealed because both Brandt and Rao teach against the combination suggested by the examiner and because the combination suggested by the examiner is based on improper hindsight reconstruction. Furthermore, applicants assert that Brandt does not teach the elements of claim 43 as suggested by the examiner.

The Combination Suggested by the Examiner is Improper

In the examiner's comments in Section 11 of the Advisory Action of November 10, 2005, the examiner stated that he did not agree that Brandt teaches away from using flash memory, as he believes that "there are as many reasons to use it as not." The examiner further stated, "It is merely a design choice based on the considerations so well known to those of even rudimentary skill in the art such as cost, size, speed, etc. Brandt simply chose the cheaper route."

However, applicant respectfully asserts that the examiner seems to be ignoring the direct intent and teaching of Brandt. Generally, Brandt's system derives its advantages from the fact that it utilizes inexpensive disk drives as opposed to expensive solid state devices. Brandt discusses the fact that the cost reduction of manufacturing disk drives has far outpaced the cost reductions associated with solid state devices. Column 1, lines 39-42. Brandt states that his invention "advantageously utilizes an array of relatively slow devices, such as low cost disk drives...." Column 2, lines 38-39.

Specifically, Brandt teaches, in Column 6, lines 3-6, that his system "*is an improvement over* directly coupling host 10 to the high volume data storage subsystem 25, or *using a solid state type device, such as caching through the use of a RAM for such interfacing*." (Emphasis added). Brandt's intent with his invention is to maximize the highest throughput performance *at the least cost* between a host computer and a mass storage system (See the Abstract, lines 2-4). Brandt states that, with this approach, "the high cost of solid state interfacing is significantly avoided by a large margin..." (Column 6, lines 9-11). Clearly, Brandt teaches the advantage of his device as being its use of relatively slow and inexpensive devices.

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to combine the teachings of these references. Therefore, based on the teachings of Brandt and of Rao, one of ordinary skill in the art would be specifically *discouraged* from replacing Brandt's multiple disk drives with non-volatile, solid state memory devices.

In establishing a *prima facie* case of obviousness under 35 USC 103, it is incumbent upon the Examiner to provide a "clear and particular" showing of "actual evidence" of a suggestion, teaching, or motivation to combine references. In re Dembiczak, 50 USPQ 2d, 1614, 1617 (Fed. Cir. 1999). "Broad conclusory statements regarding the teachings of multiple references, standing alone, are not evidence." Id., citing McElmury v. Arkansas Power and Light Co., 995 F.2d 1576, 1578, 27 USPQ2d. 1129, 1131 (Fed. Cir. 1993) (internal quotations omitted).

In the rejection, the examiner has broadly stated that Brandt teaches multiple disk drives, that Rao teaches the use of flash memory and that, based on ordinary skill in the art, it would be obvious to combine the two references to come up with applicants' invention. The examiner has not specified any teaching in either reference that would support this combination. Furthermore, the examiner seems to have ignored Brandt's direct teaching *against* the use of solid state memory, with this teaching against being supported by Rao.

In In re Dembiczak, the Court of Appeals for the Federal Circuit recognized that "rigorous application" of the requirement for a showing of a teaching or motivation to combine references is the "best defense against the subtle but powerful attraction" of improper hindsight-based obvious analysis. Id.; See also, Para-Ordnance Manufacturing, Inc. v. SGS Importers International, Inc., 73 F.3d 1085, 37 USPQ2d 1237 (Fed. Cir. 1995). ("obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor"). This is especially true in cases where the ease with which the invention may be understood "may prompt one to fall victim to the insidious effect of hindsight syndrome wherein that which only the inventor taught is used against its teacher." Id. citing W.L. Gore & Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 313 (Fed. Cir. 1983).

The examiner states that even one of rudimentary skill in the art would see that the type of memory used in Brandt is a design choice. However, the examiner has not provided any evidence in either reference or any documentary evidence to prove that, based on the teachings of Brandt and Rao, that that is the case. Only applicants' disclosure teaches the use of non-volatile memory devices in a data storage device as recited in applicants' claims. Accordingly, the only support for the examiner's position the applicants' disclosure, thus rendering the

combination relied upon by the examiner as being improperly based hindsight reconstruction. And, as set forth above, this still ignores the fact that both Brandt and Rao teach away from the combination proposed by the examiner.

Accordingly, because Brandt teaches away from utilizing any type of flash, RAM or other type of solid state memory that is not a disk drive because it is not relatively slow and inexpensive, because both Rao and Brandt support the conclusion that flash memory is expensive, and because the only basis for the combination proposed by the examiner is improper hindsight reconstruction, applicants respectfully assert that the 35 U.S.C. §103(a) rejection of independent claim 43 is improper as being based on an improper combination of references.

Brandt Does Not Teach What The Examiner Relies Upon It To Teach

Independent claim 43 recites a data storage system comprising:

at least one first data storage device having a platter size of at least 3.5 inches in diameter;

at least one second data storage device comprising:

a device interface for receiving data access requests;

a device housing conforming to a standard form factor;

a plurality of non-volatile memory devices housed within the device housing, the plurality of non-volatile memory devices being selected from the group consisting of flash memory; compact flash memory; magnoresistive RAM; ferroelectric RAM; dynamic RAM and static RAM being maintained as non-volatile with the use of a power subsystem and microelectromechanical memory devices; and

a first controller configured to receive data access requests from the device interface; and

a second controller that coordinates data access to the at least one first data storage device and the at least one second data storage device.

The examiner states that Brandt teaches at least one first data storage device having a platter size of at least 3.5 inches in diameter, as well as a second data storage device including a plurality of non-volatile memory devices. The examiner also states that Brandt teaches, in

addition to a first controller, a second controller that coordinates data access to the at least one first data storage device and the at least one second data storage device.

Regarding the first data storage device, the examiner states that, because Brandt lists different types of disk drives in column 5, he teaches that element of the claimed invention. However, applicants assert that the list only illustrates the cost/performance order of the devices. Brandt does not teach or suggest the use of *both* disk drives and non-volatile memory devices in his system, as is recited in claim 43.

Regarding the second controller, the examiner states that element 24 in Fig. 1 is the same as applicants' second controller that coordinates data access to the at least one first data storage device and the at least one second data storage device. However, as described in Column 6, line 42 of Brandt, it is clear that element 24 is simply an interface solely between controller 20 and disk system 25. This interface does not "coordinate[s] data access to the at least one first data storage device *and* the at least one second data storage device," as does the second controller 116, Fig. 7, recited in claim 43.

Accordingly, because Brandt does not teach the elements that the examiner relies upon him to teach, the combination suggested by the examiner, even if it was proper, does not teach the invention recited in claim 43.

Applicants therefore respectfully assert that independent claim 43 is allowable over the cited art of record and that the 35 U.S.C. §103(a) rejection of independent claim 43 should be withdrawn.

VIII. CLAIMS APPENDIX

30. A data storage device comprising:

a device interface for receiving data access requests;

a device housing conforming to a standard form factor;

a plurality of non-volatile memory devices housed within the device housing, the plurality of non-volatile memory devices being selected from the group consisting of flash memory; compact flash memory; magnoresistive RAM; ferroelectric RAM; dynamic RAM and static RAM being maintained as non-volatile with the use of a power subsystem and microelectromechanical memory devices; and

a controller that accesses the non-volatile memory devices in response to the received data access requests.

31. The data storage device of claim 30, wherein the interface comprises an interface configured to conform to a protocol.

32. The data storage device of claim 31, wherein the protocol comprises at least one of the following: SCSI (Small Computer System Interface), Fibre Channel, and INFINIBAND.

33. (Canceled)

34. The data storage device of claim 30, wherein the device housing conforms to at least one of the following standard form factors: full-height, half-height, and low-profile.

35. The data storage device of claim 30, wherein the controller comprises a controller configured to implement a RAID scheme.

36. The data storage device of claim 35, wherein the scheme implemented by the controller comprises a RAID scheme independent of a hierarchically higher RAID controller that sends the data storage device RAID data.

37. The data storage device of claim 30, further comprising a cache manager.

38. The data storage device of claim 37, wherein the cache manager comprises a manager configured to perform at least one of the following: translate an address of a different storage device to a cache address; cache data included in a write request; load data from the different storage device; and remove cached data.

39. The data storage device of claim 30, further comprising a controller card that includes the controller and connections available to couple with more than one storage card that provides access to the plurality of non-volatile memory devices.

40. The data storage device of claim 39, wherein the storage card comprises a card having at least one parallel interface to a collection of the drives.

41. The data storage device of claim 39, wherein the connection between the controller and the storage card comprises a serial connection.

42. The data storage device of claim 39, wherein the controller comprises a bank interface that routes data requests to an appropriate bank of drives.

43. A data storage system comprising:

at least one first data storage device having a platter size of at least 3.5 inches in diameter;

at least one second data storage device comprising:

a device interface for receiving data access requests;

a device housing conforming to a standard form factor;

a plurality of non-volatile memory devices housed within the device housing, the plurality of non-volatile memory devices being selected from the group consisting of flash memory; compact flash memory; magnoresistive RAM; ferroelectric RAM; dynamic RAM and static RAM being maintained as non-volatile with the use of a power subsystem and microelectromechanical memory devices; and

a first controller configured to receive data access requests from the device interface; and

a second controller that coordinates data access to the at least one first data storage device and the at least one second data storage device.

44. (Canceled)

45. A method of servicing data access requests at a data storage device, the method comprising:

receiving data access requests at a device interface of the data storage device; and

accessing a plurality of non-volatile memory devices housed within a standard form factor device housing in response to the received data access requests, the plurality of non-volatile memory devices being selected from the group consisting of flash memory; compact flash memory; magnoresistive RAM; ferroelectric RAM; dynamic RAM and static RAM being maintained as non-volatile with the use of a power subsystem and microelectromechanical memory devices.

46. (Canceled)

47. A data storage device comprising:

a device interface for receiving data access requests;

a plurality of non-volatile memory devices, the plurality of non-volatile memory devices being selected from the group consisting of flash memory; compact flash memory; magnoresistive RAM; ferroelectric RAM; dynamic RAM and static RAM being maintained as non-volatile with the use of a power subsystem and microelectromechanical memory devices; and

a controller that accesses the non-volatile memory devices in response to the received data access requests;

wherein the controller comprises a controller configured to implement a RAID scheme.

48. The data storage device of claim 47, wherein the scheme implemented by the controller comprises a RAID scheme independent of a hierarchically higher RAID controller that sends the data storage device RAID data.

49. A data storage device comprising:

a device interface for receiving data access requests;

a plurality of non-volatile memory devices; and

a controller that accesses the non-volatile memory devices in response to the received data access requests;

wherein the plurality of non-volatile memory devices include at least one of flash memory; compact flash memory; magnoresistive RAM; ferroelectric RAM; any type of volatile memories, such as dynamic and static RAM, maintained as non-volatile with the use of a power subsystem; and microelectromechanical memory devices.

50. A data storage device comprising:

a device interface for receiving data access requests;

a plurality of non-volatile memory devices, the plurality of non-volatile memory devices being selected from the group consisting of flash memory; compact flash memory; magnoresistive RAM; ferroelectric RAM; dynamic RAM and static RAM being maintained as non-volatile with the use of a power subsystem and microelectromechanical memory devices; and

a controller that accesses the non-volatile memory devices in response to the received data access requests;

wherein the controller is configured to access the non-volatile memory devices in a manner that emulates access to a single disk drive.

IX. EVIDENCE APPENDIX

A. U.S. Patent No. 5,805,787 to Brandt et al., entitled Disk Based Disk Cache Interfacing System and Method
Cited by the examiner in the Office Action dated March 9, 2005.

B. U.S. Patent No. 5,845,104 to Rao, entitled Method And System For Reading Data From And Writing Data To A Jukebox Using A Cache
Cited by the examiner in the Office Action dated June 17, 2005.